

## ABSTRACT OF THE DISCLOSURE

An embodiment of the invention is a dual damascene layer 13 of an integrated circuit 2 containing a dual damascene pattern liner 21. Another embodiment of the invention is a method of manufacturing dual damascene layer 13 where a dual damascene pattern liner 21 is formed over a cap layer 25 and within via holes. Yet another embodiment of the invention is a method of manufacturing dual damascene layer 13 where a dual damascene pattern liner 21 is formed over a cap layer 25 and within trench spaces.